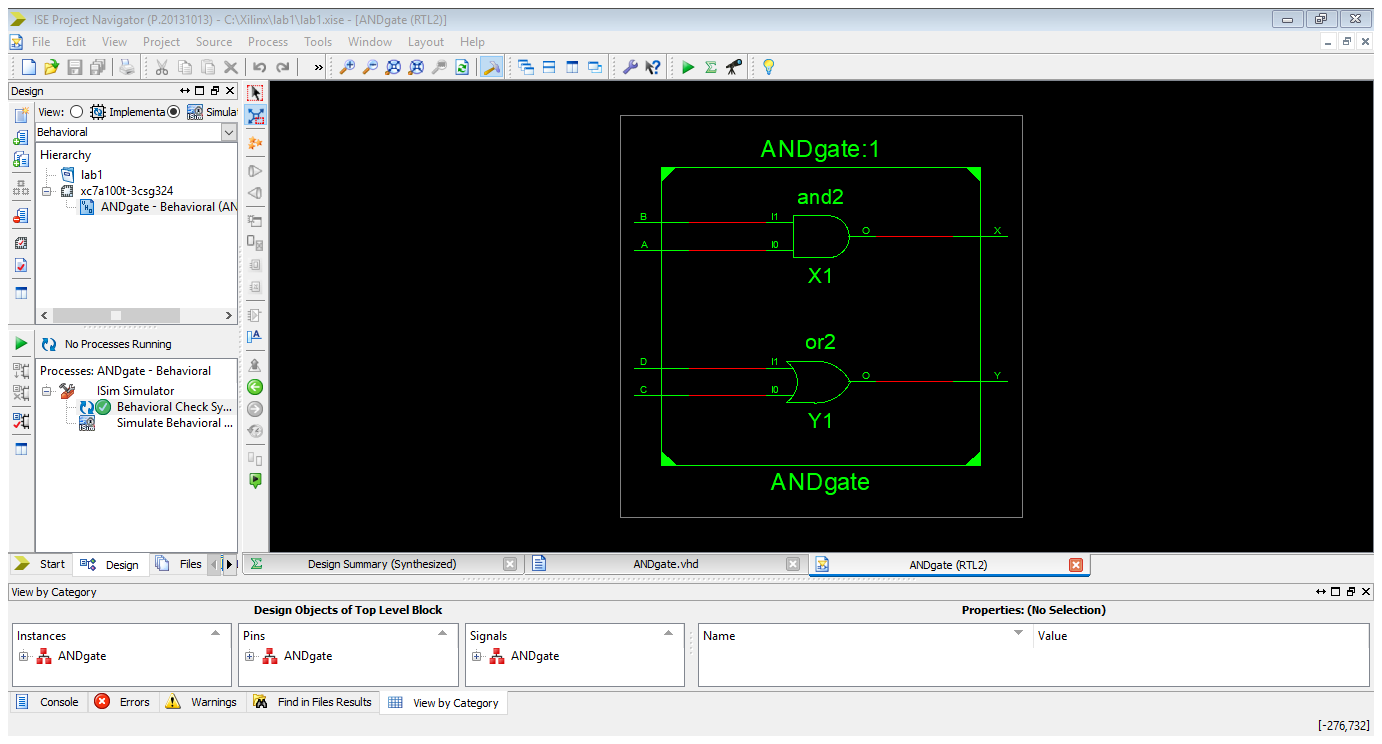
**LAB 1**

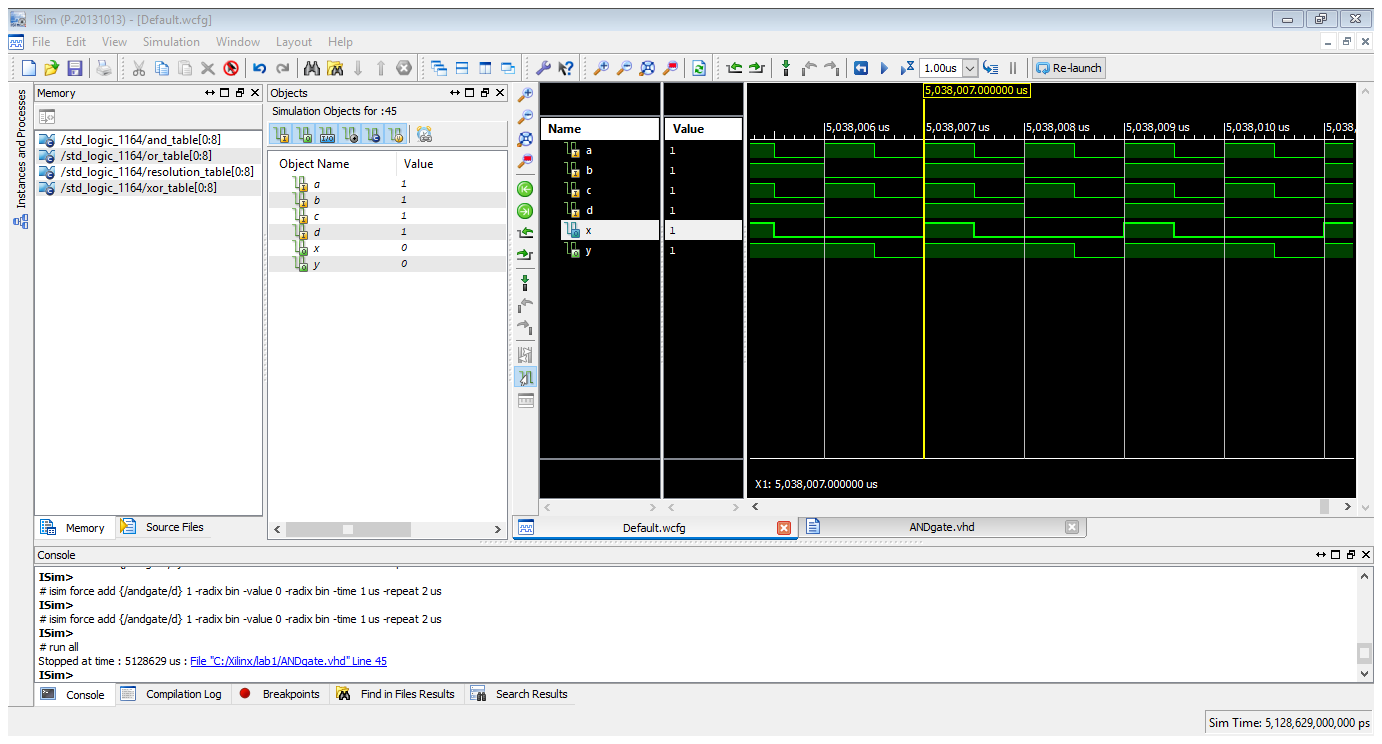
**GROUP MEMBERS:-** Shahrukh Padaniya (C0769542)

Rohan Yadav (C0773871)

Swapnil Sevak (C0777195)

**Schematics: -**



**Simulation: -** 

**Truth Table: -**

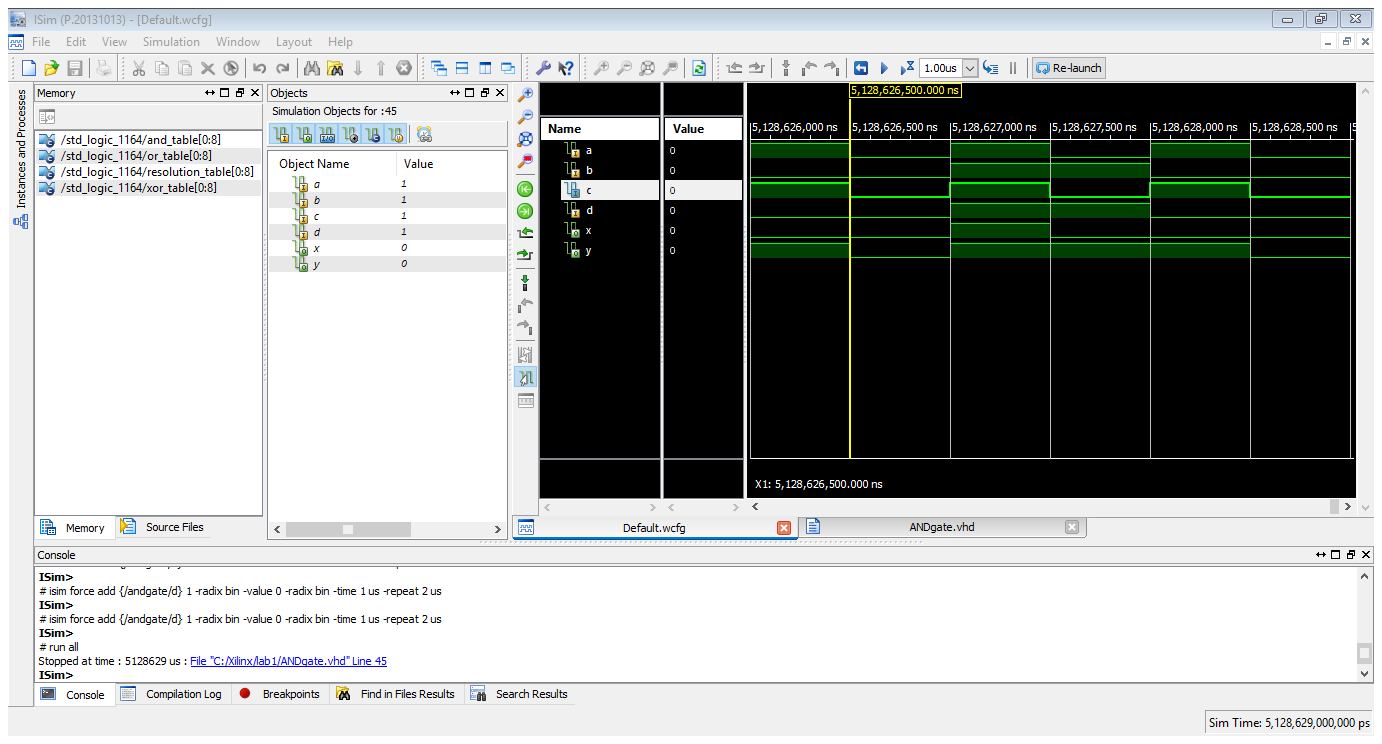
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **X=A.B** | **Y=A+B** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

**CASE-1: -**

A,B,C,D = 0

X=A.B = 0

Y=C+D = 0

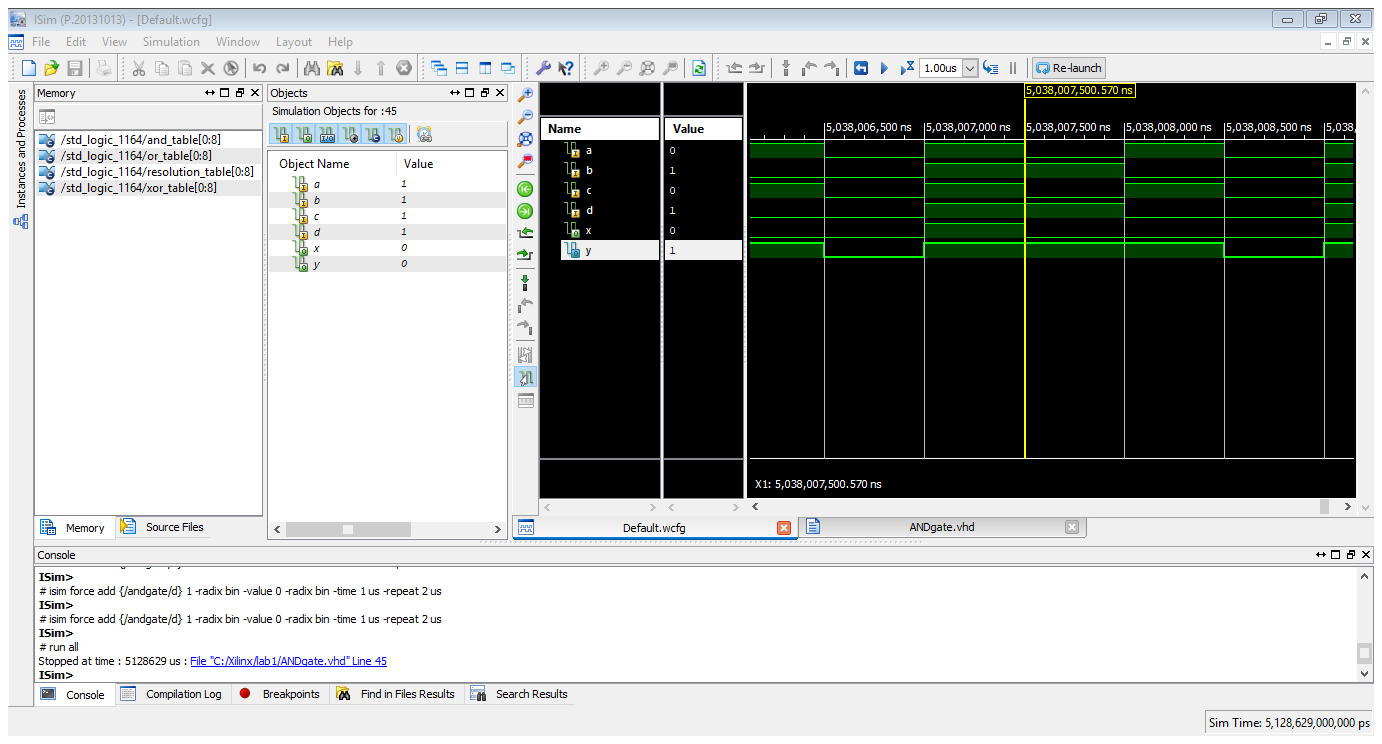


**CASE-2: -**

A,C=0 B,D=1

X=A.B = 0

Y=C+D = 1

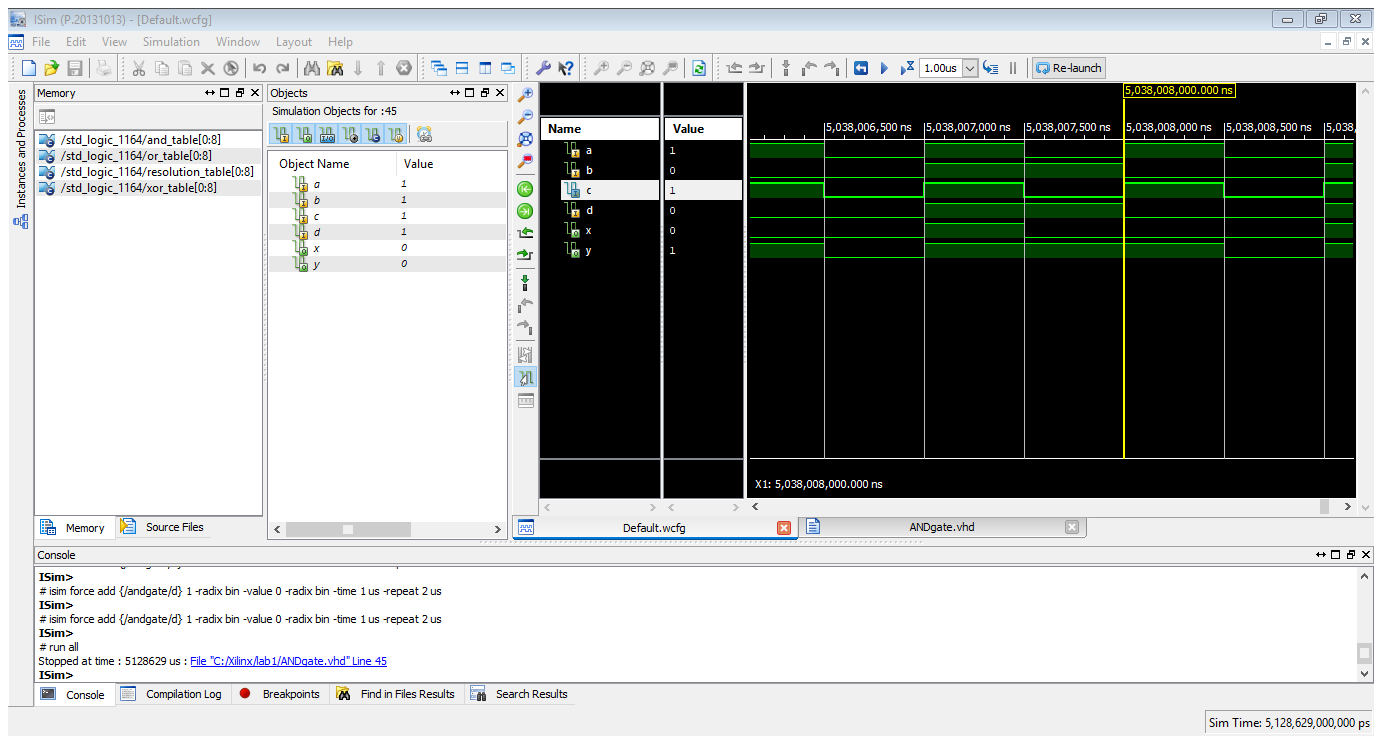


**CASE-3: -**

A,C=1 B,D=0

X=A.B = 0

Y=C+D = 1

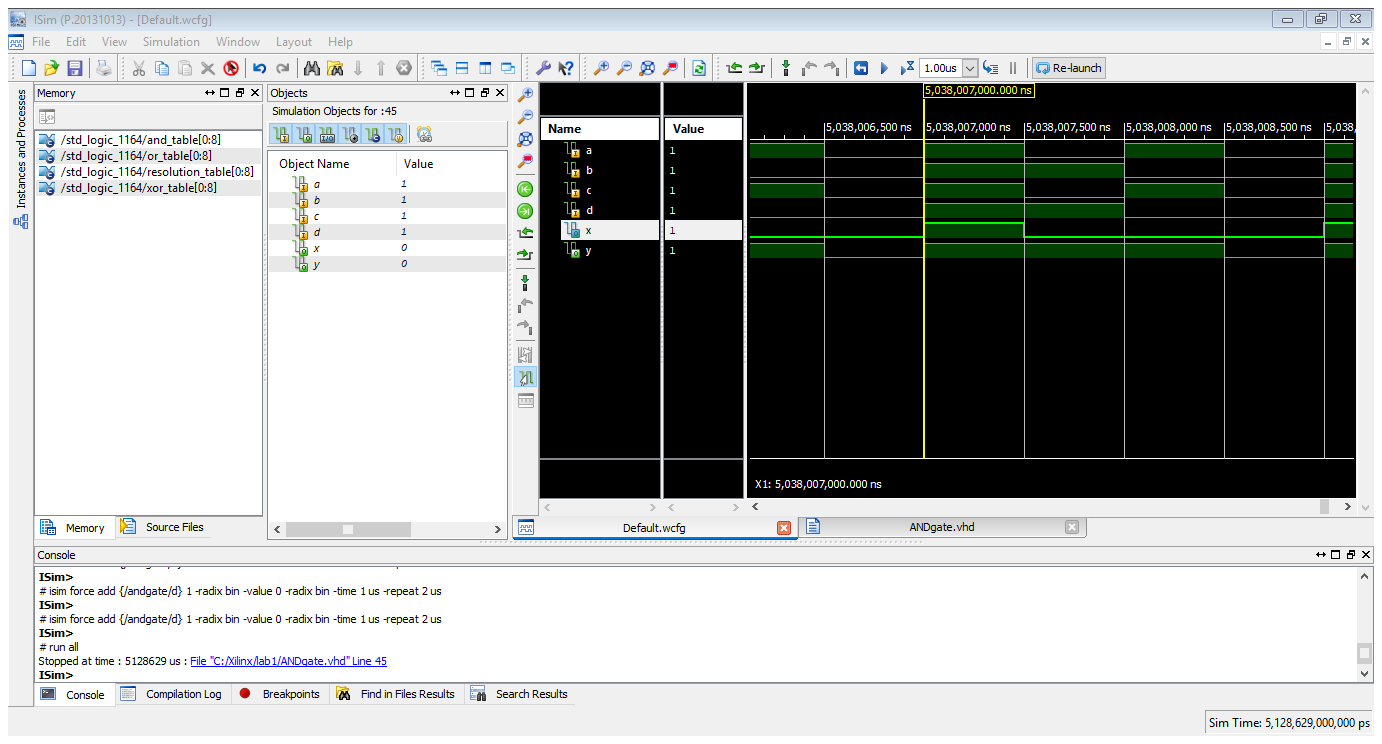


**CASE-4: -**

A,B,C,D=1

X=A.B = 1

Y=C+D = 1



**XILINX CODE: -**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity ANDgate is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : in STD\_LOGIC;

D : in STD\_LOGIC;

X : out STD\_LOGIC;

Y : out STD\_LOGIC);

end ANDgate;

architecture Behavioral of ANDgate is

begin

X <= A AND B;

Y <= C OR D;

end Behavioral;